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10/623,559	07/22/2003	Yoshihisa Iwata	240522US2S	6040

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/623,559	IWATA, YOSHIHISA	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-14 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-14,23 and 24* is/are allowed.

6)☒ Claim(s) *16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in Fig.1 in view of Kikuchi (U. S. PAT. 6,151,150).

In claim 16, the AAPA in Fig. 1 teaches a signal transmission system which transmits and receives binary logic signals (logic 1 and logic 0) between a plurality of semiconductor apparatuses (100s), wherein the plurality of semiconductor apparatuses respectively have an input receiver (100 in Fig. 1 of AAPA) that is connected to a signal transmission line (one of lines 11 in fig. 1), and the input receiver decides a logic level of an external input signal (Vin in Fig. 2) input from the signal transmission line; with the exception of teaching a first and a second reference voltages. However, Kikuchi teaches in Figs. 7-8, a first reference signal (V_{pk1}) corresponding to a logic "1" level (Fig. 8) of the input signal (Vin) and a second reference signal (V_{pk2}) corresponding to a logic "0" level (Fig. 8) are supplied as reference signals for logic level decision (30 in Fig. 7) to the respective input receivers, and the respective input receivers output on of the logic "1) level and the logic "0" level, and the output of the respective input receivers follows the external signal (Vout); with the exception of teaching wherein the first and second reference signals are inputted from outside of the plurality of semiconductor

apparatus. However, it would have been obvious to one ordinary having skill in the art at the time the invention was made to have the first and second reference signals inputted from outside of the plurality of semiconductor apparatus instead from inside, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japiske*, 86 USPQ 70.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to combine the teachings of the AAPA in Figs 1 and 2 with the teachings of Kikuchi in order to provide detection circuits that can be used for transmitting signals in semiconductor circuits such as memory devices.

In claim 17, the AAPA in fig. 1 further teaches the plurality of semiconductor apparatuses (100s) are packaged on a same wiring board (Fig. 1), and structure a semiconductor module (as seen in Fig. 1).

In claim 18, Kikuchi further teaches the signal transmission system of claim 16, wherein each of the input receivers including: a first comparison circuit (35) which compares an input signal (Vin) with a first reference signal (V_{pk1}) corresponding to logic "1" level, and which outputs a first differential signal (Vsum2); a second comparison circuit (34) which compares the input signal (Vin) with a second reference signal (V_{lpk2}) corresponding to logic "0" level, and which outputs a second differential signal (Vsum1); and a third comparison circuit (36) which compares output of the first comparison circuit and output of the second comparison circuit, and which decides a logic level (logic 1 or logic 0) of the input signal.

In claim 19, Kikuchi further teaches the signal transmission system according to claim 16, wherein a signal level (a voltage level) of the first reference signal (V_{pk1}) is greater (higher) than a signal level (a voltage level) of the second reference signal (V_{pk2}), and the signal level of the first reference signal is a value greater than a maximum value (highest voltage level for Vin) of a distribution of a signal level of the logic "1" level of the input signal (Vin), and the signal level of the second reference signal is a value less than a minimum value (lowest voltage level) of a distribution of a signal level of the logic "0" level of the input signal (Vin).

Claim 20 is rejected in the same manner as claim 19, by reversing the first reference signals V_{pk1} and V_{pk2} around.

3. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi.

In claim 21, Kikuchi teaches all claimed features in Figs. 7 and 8, a semiconductor apparatus comprising a logic level decision circuit (30) that is connected to a signal transmission line (a line that coupled to INPUT), the logic level decision circuit having a first reference signal (V_{pk1}) having a logic "1" level and a second reference signal (V_{pk2}) having a logic "0" level input as reference signals for deciding a logic level of an input signal (Vin) input from the signal transmission line, and which decides the logic level of the input signal in accordance with which of the signal levels of the first and second reference signals the signal level of the input signal is close to; with the exception of teaching wherein the first and second reference signals are inputted from outside of the plurality of semiconductor apparatus. However, it would have been

obvious to one ordinary having skill in the art at the time the invention was made to have the first and second reference signals inputted from outside of the semiconductor apparatus instead from inside, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japiske*, 86 USPQ 70.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to have the first and second reference signals inputted from outside of the semiconductor apparatus instead from inside, in order to easily gain access in an event that the reference signals need adjustments.

In claim 22, Kikuchi teaches all claimed features in Figs. 7 and 8, a semiconductor apparatus having a logic level decision circuit (30), the logic level decision circuit comprising: a first comparison circuit (35) which compares an external input signal (Vin) of a signal transmission line (a line that coupled to INPUT) with a first reference signal (V_{pk1}) corresponding to logic "1" level, and which outputs a first differential signal (Vsum2); a second comparison circuit (34) which compares the external input signal with a second reference signal (V_{pk2}) corresponding to logic "0" level, and which outputs a second differential signal (Vsum1); and a third comparison circuit (36) which compares the output of the first comparison circuit and the output of the second comparison circuit, and which outputs one of the logic "1" level and the logic "0" level, wherein the output of the third comparison circuit (Vout) follows the external input signal (in Fig.8); with the exception of teaching wherein the first and second reference signals are inputted from of the semiconductor apparatus. However, it would have been obvious to one ordinary having skill in the art at the time the invention was

made to have the first and second reference signals inputted from outside of the semiconductor apparatus instead from inside, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japiske*, 86 USPQ 70.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to have the first and second reference signals inputted from outside of the semiconductor apparatus instead from inside, in order to easily gain access in an event that the reference signals need adjustments.

4. Claims 9-14, 23 and 24 appear to comprise allowable subject matter of the first comparison circuit is a current mirror type first voltage comparison circuit, and the second comparison circuit is a current mirror type second voltage comparison circuit.

Response to Arguments

5. Applicant's arguments with respect to claims 16-22 have been considered but are moot in view of the new ground(s) of rejection.

Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA) in Fig.1 in view of Kikuchi; and claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi, as set forth in above detailed action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VIBOL TAN
PRIMARY EXAMINER